Serial No. 10/056,610
Docket No. – MIO 0051 V2

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

Please amend claim 30 as follows:

1-29. (canceled)

30. (currently amended) A method of encapsulating an integrated circuit comprising the steps of:

providing a semiconductor chip;

providing a laminate defining first and second major faces, said laminate including an electrically conductive layer, and an underlying substrate supporting said electrically conductive layer;

forming at least one void in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

encapsulating said semiconductor ~~die~~chip and said laminate with an encapsulant such that said encapsulant extends into said void to contact said underlying substrate.

31. (canceled)

32. (original) A method of forming a laminate to lock an encapuslant comprising:

providing a first laminate layer;

forming a second laminate layer over the first laminate layer, so as to define an underlying cavity;

forming a third laminate layer over the second laminate layer, so as to define a void portion over the underlying cavity;

forming a fourth laminate layer over the third laminate layer, so as to define a void portion over the void portion of the third laminate layer;

forming a conductive layer over the fourth laminate, so as to define a void portion over the void portion of the fourth laminate layer; and

forming a solder resist layer over the conductive layer, so as to define a void portion over the void portion of the conductive layer.

33. (original) The method of claim 32, wherein the underlying cavity, the void portion of the third laminate layer, the void portion of the fourth laminate layer, the void portion of the conductive layer and the void portion of the solder resist layer are formed to collectively form a void.

34. (original) The method of claim 33 further comprising:

placing a die over at least a portion of the solder resist layer;

forming an encapsulant over the solder resist layer, over the die and in the void.

35–39. (canceled)

40. (original) A method of encapsulating an integrated circuit comprising:

providing a die;

providing a substrate having at least one resin layer;

forming at least one laminate layer over the at least one resin layer;

forming a void in the at least one resin layer and the at least one laminate layer such that a portion of the void located in the at least one resin layer is below a remaining portion of the at least one laminate layer;

placing the die over the at least one laminate layer; and

encapsulating the die by forming encapsulant over the at least one laminate layer, over the die and in the void.

41. (original) The method of claim 40, wherein the at least one laminate layer is formed by forming a conductive layer over the at least one resin layer and forming a solder resist layer over the conductive layer.

42. (original) The method of claim 40, wherein the void is formed by forming an underlying cavity in the at least one laminate layer.

43. (original) The method of claim 40, wherein the encapsulant is formed in substantially all of the void.

44. (original) The method of claim 40, wherein the at least one resin layer is formed from bismaleimide triazine laminate.

45. (original) The method of claim 40, wherein the at least one resin layer is formed from FR-4 epoxy-glass laminate.

46-49. (canceled)

50. (previously presented) The method of claim 33, wherein the void has a varying profile.

51. (previously presented) The method of claim 50, wherein the void having a varying profile is formed by a process selected from the group consisting of drilling, stamping, chemical etching, and combinations thereof.

52. (previously presented) The method of claim 50, wherein the void having a varying profile is formed having a T-shaped profile.